

Amendments to the Specification:

Please replace paragraph [0041] with the following amended paragraph.

[0041] An n-type JFET region 320 is disposed in an upper portion of the n⁻-type epitaxial layer 306 using conventional processing techniques. The n-type JFET region 320 forms a pn junction 321 with the p⁻-type well region 308. The impurity concentration of the n-type JFET region 320 is higher than that of the n⁻-type epitaxial layer 306. A p⁻-type floating well region 322 is also disposed in an upper portion of the n⁻-type epitaxial layer 306 using conventional processing techniques. The n-type JFET region 320 forms a second pn junction 321 323 with the p⁻-type floating well region 322. The p⁻-type floating well region 322 is spaced apart from the p⁻-type well region 308 by the n-type JFET region 320. In a 600V IGBT embodiment, a distance between the p⁻-type floating well region 322 and the p⁻-type well region 308 is approximately 3 μ m to 6 μ m and becomes longer with an increase in the device voltage rating.

Please replace paragraph [0045] with the following amended paragraph.

[0045] In all three variations, as shown in FIGS. 4A through 4C, a substantially similar pattern of hole current distribution can be observed uniformly distributed. That is, most hole current moves through a junction between the n⁻-type epitaxial layer 306 and the p⁻-type well region 308. In particular, most hole current flows through the bottom of the p⁻-type well region 308 with the largest area. This is because the p⁻-type floating well region 322 suppresses the occurrence of breakdown at the surface of the device. If the p⁻-type floating well region 322 is not formed, a relatively high concentration of impurity ions in the n-type JFET region 320 causes an electric field crowding. Thus, as described above, breakdown occurs at the surface of the device and a large amount of current flows along the surface and channel region 309.